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09/008,531	01/16/1998	HOWARD E. RHODES	MIO012V2	6336

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EXAMINER
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ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/008,531	Applicant(s) RHODES, HOWARD E.	
	Examiner Michael M Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/8/02 & 9/27/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-32,35,36,40-43 and 48* is/are pending in the application.

4a) Of the above claim(s) *26-30,35,36,40-43 and 48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-25,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's election filed on May 08. 2002, and Amendment filed on 9/27/01. Claims 21-32,35,36,40-43,48 are currently pending, in which claims 26-30,35-36,40-43,48 are non-elected invention.

Election/Restrictions

1. Applicant's election filed 5/8/02 with traverse of method claims 21-25,31-32 in Paper No. 26 is acknowledged, in which recently added claims 26-30,35-36,40-43,48 are non-elected invention. The traversal is on the ground(s) that "the claims are all generally related to a process for making a semiconductor device...review of all of the claims in a single application would not necessitate an extensive further search nor be unduly burdensome for the Examiner". This is not found persuasive because, as already shown these inventions are species and distinct for the reasons as given in the restriction requirement and have acquired a separate status, in which the fields of search are not co-extensive and separate examination would be required for these distinct inventions. It is the fact that Applicant did not distinctly and specifically point out the supposed errors of the given reasons in the restriction requirement, in which separate examination would be required. Examining and searching these multiple distinct and species inventions clearly indicate that there is a very serious burden on the examiner and to the Office. Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Restriction for examination purposes as indicated is proper.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 26-30,35,36,40-43,48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 112

3. Claims 31-32 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

It is noted that original specification teaches to form a structure having an opening, then filling the opening with a conductive material to form a conductive layer.

Base claim 31, last step recites "forming a structure having an opening therein **under** said conductive layer...". However, for a process claim and in the order of step recitation, it is new matter since original specification does not teach to form a conductive layer (as recited at second step), then forming the opening **under** the conductive layer (as recited at last step).

Apparently, the last step should be amended and recited before second step of forming a conductive layer.

(Dependent claim 32 is rejected as depending on rejected base claim 31)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 21-24,31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Zamanian (5,793,111).

Zamanian teaches, at Figures 1-6 and cols 3-6, a method for forming a semiconductor device comprising at least the steps of: providing a substrate having at least one semiconductor layer 10; forming an underlayer 28 (Fig 2) over the at least one semiconductor layer 10; forming

a layer of conductive material 32/34/36 over the underlayer 28 having a topography that includes a substantially vertical component (Figs 3) and defining a localized thick region; forming an overlayer 40 over said layer of conductive material; etching to form a contact hole in the overlayer 40 and in an overetch amount of the substantially vertical component (Fig 6; col 5, line 50 through col 6); and forming a contact 44 in said contact hole disposed adjacent to, in the vertical component, and contacting the vertical component (Fig 6).

Re claims 22 and 32, Zamanian shows the vertical component defining a localized thick region in the layer of conductive material.

Re claim 23, Zamanian shows wherein layer of conductive material having the vertical component formed as a spacer.

Re claim 24, Zamanian forms a structure 28 having an opening therein under the conductive layer and filling the opening with the conductive material to form the vertical component.

6. Claims 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada (5,399,890).

In re claim 31, Okada shows in Figures 2A-2C,3 and related text (col 6, lines 27 through col 8, line 8), a method for making a semiconductor device including the steps of: providing a substrate having at least one semiconductor layer 1; forming a layer of conductive material (9 in Fig 2C; or 9b/9a in Fig 3) having a topography that includes a substantially vertical component defining a localized thick region; forming an overlayer 10 over said layer of conductive material (col 7, lines 1-12); and forming a contact 12 in said overlayer 10 and in the vertical component disposed adjacent to and contacting the vertical component of the layer of conductive material 9, wherein the method includes forming a structure having an opening therein and filling the opening with conductive material to form the conductive layer above the opening having the vertical component

Re claim 32, Okada shows the vertical component defining a localized thick region in the layer of conductive material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 21-25,31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al (5,312,769) taken with Zamanian (5,793,111) and Wolf (pages 547-554).

In re claims 21, and 31, Matsuo shows in Figures 2A-2E and related text, a process for making a semiconductor device including the steps of providing a substrate having at least one semiconductor layer 1; forming an underlayer 21 over the at least one semiconductor layer; forming a layer of conductive material 12 over the underlayer 21 having a topography that includes a substantially vertical component defining a localized thick region; forming an overlayer over said layer of conductive material; forming contact hole in the overlayer and in an overetch amount of the substantially vertical component; and forming a contact in said contact hole disposed adjacent to and contacting the vertical component. Matsuo also shows wherein the contact hole window 29 is formed in the first interlayer insulating film 23 formed by using a dry etching technique (see Figure 2B; column 5, lines 30-46). Matsuo further shows in Figure 2B wherein the overlayer is made of oxide material and wherein the layer of conductive material is made of polysilicon (col 3, line 59 through col 5, line 55).

Matsuo fails to show etching in an overetch amount of the substantially vertical component.

However, Zamanian teaches (at Fig 6,1-5; col 5, line 50 through col 6, lines 22; cols 3-5) that in order to insure that all of the dielectric has been removed from the contact opening, etching a contact hole in the overlayer 40 and in an overetch amount of the layer of conductive material having a substantially vertical component. Wolf teaches that eventhough the oxide material is etched selectively to polysilicon material, some tolerable amount of polysilicon material is etched as well (pages 547-554).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Matsuo et al (Figure 2B) by etching a contact hole in the overlayer insulator 23 and in an overetch amount of the layer 12 of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Wolf, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact.

Re claims 22 and 32, Matsuo et al shows the vertical component defining a localized thick region in the layer of conductive material.

Re claim 23, Matsuo shows wherein the vertical component is a spacer.

Re claim 24, Matsuo forms a structure 21 having an opening therein under the conductive layer 12 and filling the opening with the conductive material to form the vertical component.

Re claim 25, Matsuo shows wherein the contact 13 disposed adjacent to and contacting the vertical component 12 is a storage capacitor electrode made of the same material as the layer of conductive material (column 4, lines 3-22), in which the layer of conductive material is considered a part of the capacitor electrode.

8. Claims 21-25,31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al (5,399,890) taken with Zamanian (5,793,111) and Toshiyuki et al (JP-05-109905).

In re claims 21, and 31, Okada shows in Figures 2A-2C,3 and related text (col 6, lines 27 through col 8, line 8), a method for making a semiconductor device including the steps of: providing a substrate having at least one semiconductor layer 1; forming an underlayer 8 (Fig 2C) over the at least one semiconductor layer 1; forming over the underlayer, a layer of

conductive material (9 in Fig 2C; or 9b/9a in Fig 3) having a topography that includes a substantially vertical component defining a localized thick region; forming an overlayer 10 over said layer of conductive material (col 7, lines 1-12); etching to form a contact hole 11 in the overlayer 10 and over the substantially vertical component; and forming a contact 12 in said contact hole 11 disposed adjacent to, and contacting the vertical component of the layer of conductive material 9.

Okada et al fails to show etching in an overetch amount of the substantially vertical component.

However, Zamanian teaches (at Fig 6,1-5; col 5, line 50 through col 6, lines 22; cols 3-5) that in order to insure that all of the dielectric has been removed from the contact opening, etching a contact hole in the overlayer 40 and in an overetch amount of the layer of conductive material having a substantially vertical component. Toshiyuki et al (JP-05-109905) teaches (at Figs 1-4; English abstrat and Computer-English Translation pages 1-3) forming a layer of conductive material 2 over an underlayer (Fig 2); forming an overlayer 3 over said layer of conductive material (Fig 2); etching to form a contact hole 9 in the overlayer 3 and in an overetch amount of the layer of the conductive material (Fig 3,1); and forming a contact 6,8 (Figs 1,4) in said contact hole 9 disposed adjacent to, in the layer of conductive material, and contacting the layer of conductive material 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Okada et al by etching a contact hole in the overlayer insulator and in an overetch amount of the layer of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Toshiyuki, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact. This is also because of the desirability to improve reliability in the multilayer interconnection structure, and to suppress occupied area of a contact part between top and bottom wiring patterns.

Re claims 22 and 32, Okada et al shows the vertical component defining a localized thick region in the layer of conductive material.

Re claim 23, Okada shows wherein the vertical component is a spacer.

Re claim 24, Okada forms a structure 8 having an opening therein under the conductive layer and filling the opening with the conductive material to form the vertical component.

Re claim 25, Okada shows wherein the conductive layer 9 is a capacitor electrode (col 6, lines 1-10).

Response to Argument

9. Applicant's remark filed September 27, 2001 have been considered but they are in moot of new ground of rejections.

Applicant's remark (at 9/27/01 remark page 5) that "the tolerable amount of overetching recited in the present invention is much higher than the amount taught in Wolf".

In response, this is noted and found unconvincing since the claimed invention as in elected claims 21-25,31-32 does not even require such overetch amount.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner